## DESCRIPTION

ValueRAM's KVR21R15D4/16 is a 2G x 72-bit (16GB) DDR4-2133 CL15 SDRAM (Synchronous DRAM) registered w/ parity, 2Rx4, ECC, memory module, based on thirty-six 1G x 4-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR4-2133 timing of 15-15-15 at 1.2V. Each 288-pin DIMM uses gold contact fingers. The electrical and mechanical specifications are as follows:

SPECIFICATIONS

| CL(IDD) | 15 cycles |
| :--- | :--- |
| Row Cycle Time (tRCmin) | $47.05 \mathrm{~ns}(m i n)$. |
| Refresh to Active/Refresh <br> Command Time $1 \times$ mode (tRFCmin) | $260 \mathrm{~ns}(m i n)$. |
| Row Active Time (tRASmin) | $33.00 \mathrm{~ns}(m i n)$. |
| Maximum Operating Power | TBD W* |
| UL Rating | $94 \mathrm{~V}-0$ |
| Operating Temperature | $0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature | $-55^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$ |

*Power will vary depending on the SDRAM used.

- Power Supply: VDD=1.2V (1.14V to 1.26 V )
- $\mathrm{VDDQ}=1.2 \mathrm{~V}(1.14 \mathrm{~V}$ to 1.26 V$)$
- VPP - 2.5V (2.375V to 2.75 V )
- VDDSPD=2.25V to 2.75 V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

MODULE DIMENSIONS


Front


